Understanding and Reducing Copper Defects

Most high-performance logic manufacturers are by now developing, piloting or producing copper-based circuits. There are a number of companies that introduced copper at the 0.18 µm device node to receive early learning. Such a strategy has helped define and refine process flows and integrated technology while the interconnect features were fairly easy to build (i.e. PVD barrier/seed, electrofill and CMP processes are straightforward to optimize). As feature sizes shrink with 0.13 and 0.10 µm design rules, several changes are required to successfully metalize such structures, which, in turn, can have a negative effect on subsequent processing.

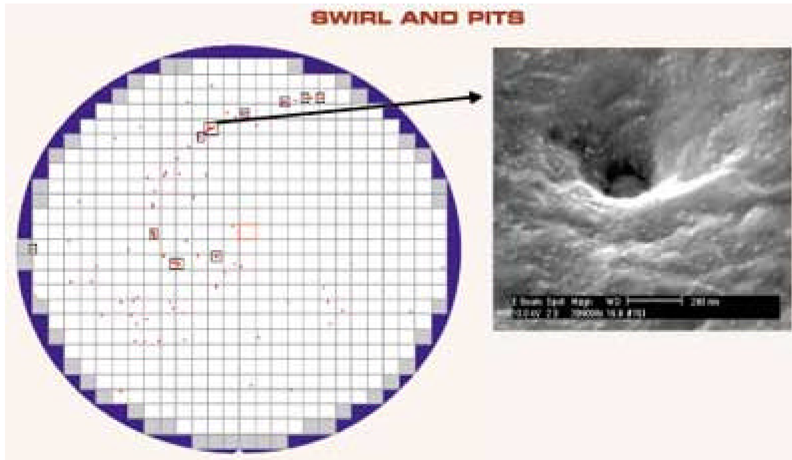
Definition of defects

In the copper deposition sequence, there are three main areas where defects can be introduced and have an impact on yield: 1) during barrier/seed deposition (in a PVD tool); 2) during electrofill; and 3) during CMP.

Defects introduced in the barrier/seed deposition step are straightforward to identify and address, provided that the appropriate metrology is applied. To this end, close collaboration with the suppliers of metrology equipment has been critical in developing analytical techniques for copper films. Similarly, the ability to analyze and monitor defects on plated films has required optimized metrology methods to lead to consistent results. Measuring copper is difficult, in part, because of its highly reflective surface and large grain size. Early attempts at measuring copper defects consisted of a trade-off between sensitivity and signal-to-noise.

To overcome false readings resulting from this high reflectivity, the instrument sensitivity would be reduced, resulting in a very low and inaccurate defect count.

Our experience here has led us to primarily use an optical contrast technique as in the KLA-Tencor AIT II system, which is very sensitive, particularly with films thinner than 1 µm. Combined with a defect review capability (optical microscope or SEM), this approach has been very powerful in classifying and addressing defects in a systematic manner.



1. The “swirl” mark is a series of pit defects that follow the arc of rotation of the wafer during plating. It is unique to the electrofill process.

In addition to copper deposition, post-electrofill processing can affect defectivity. Thermal annealing after copper deposition can aggravate the number of defects observed post-CMP if the anneal conditions are not optimal. Several types of defects are observed post-CMP that can be attributed directly to the CMP process or to the preceding steps (barrier/seed, electrofill and anneal). Because all the above defects can have a yield impact, they will be addressed individually.

Post-plating defects

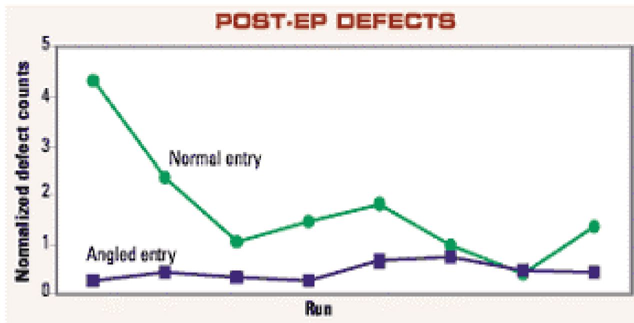
One of the in-film defects unique to the electrofill process is a "swirl" mark (Fig. 1), a series of pit defects that follow the wafer's arc of rotation during plating. Such a defect type is typically associated with incomplete wetting of the copper seed surface during the early stages of plating, resulting in dry spots or bubbles on the surface. As plating proceeds around such a bubble (ranging in size from 0.1 µm to several tens of microns), a circular defect is formed. Factors that contribute to or influence the occurrence of such defects, and that affect the wetting of the surface in the plating solution, include:

- Copper seed age or oxidation state.
- Additives in the chemistry that are strong surfactants.
- Flow dynamics of introducing a (dry) wafer into solution and the onset of plating.

The first factor is not only a function of the time between seed deposition and plating, but also the specific deposition equipment (PVD vacuum quality, cleanliness of the loadlocks, especially

during venting, etc.). Some users have resorted to imposing a time window between seed deposition and plating to get consistent results.

The second factor, chemistry, usually cannot be freely modified to address this defect issue — the overriding requirements for chemistry are the fill capability and material properties. However, some additives used for meeting the fill and uniformity requirements tend to act as good surfactants, which help improve wetting and reduce these pit defects.



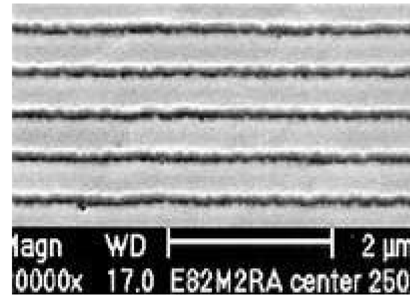
2. Reduced defect counts were obtained through characterization and modeling, and minor changes in the flow pattern and wetting step.

The third factor is mostly dependent on the plating hardware design, so can be optimized to deliver consistent, uniform wetting of the copper-seeded wafers in the plating electrolyte. This is an area where Novellus has demonstrated an impact with the Sabre xT electrofill system. An early design of the plating cell configuration resulted in inconsistent wafer surface wetting, leading to highly variable pit defect counts. That design was more susceptible to variability in the seed age as well. Through careful characterization and modeling, some minor changes in the flow pattern and wetting step (the action of inserting a wafer into solution) resulted in dramatic reductions in defect counts (Fig. 2).

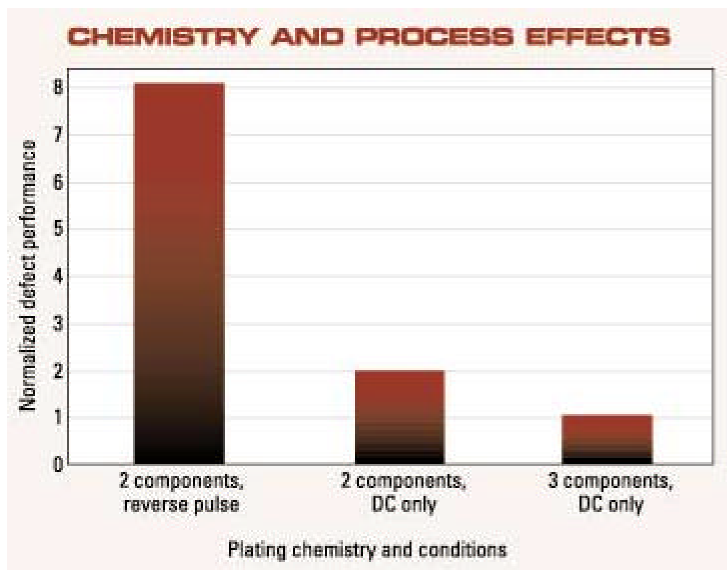
Post-CMP defects

Although post-plating defects may have a yield impact, this relationship is difficult to establish. Not all wetting-related defects result in line opens or shorts on the interconnect structures, especially if they are situated in the field (non-active) areas of the wafer. Also, damascene trenches and vias act as good capillaries, and can assist the wetting inside features. Post-CMP defects, however, can more easily be correlated to yield loss, as scratches, missing metal and remaining metal can be linked to opens and shorts. Although a number of defect types are attributed primarily to the CMP process (e.g. scratches), there are others that are simply "revealed" or "enhanced" during CMP, while they originated in one of the preceding steps. For example, an incompletely filled structure may not be detecting post-plating if the overburden has completely covered the underlying defect. Such a defect may be more easily observed post-CMP.

One of the key areas has been a defect type called a "mousebite" (Fig. 3), which effectively is missing metal that is typically on one edge of an interconnect. It is believed that this defect results from an interaction between the plating and the CMP process. Although a direct observation or confirmation has not been possible to date, one hypothesis is that this defect is created or "enhanced" during the final steps of CMP. At this point in the process, copper has been cleared from the field, exposing the underlying (Ta or TaN) barrier. Thus both copper (in the lines) and Ta (or TaN) in the field are exposed in the presence of a slurry, resulting in galvanic-enhanced corrosion. Changes in the slurry pH have shown that these defects can be modulated. Likewise, changes in the barrier material (TaN vs. Ta) have also modulated this defect to some extent, offering supporting evidence of this hypothesis.



3. A "mousebite" defect is where metal is missing, typically on one edge of an interconnect.

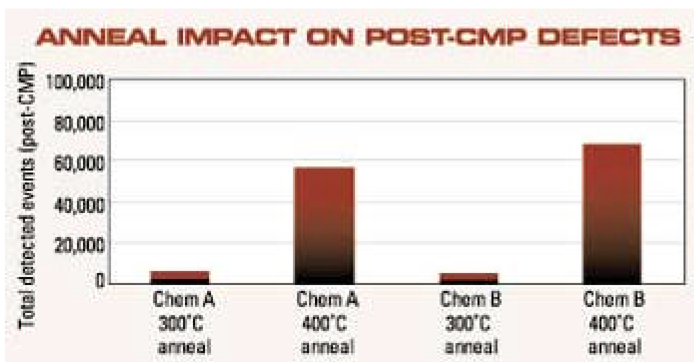


4. Post-plating anneal conditions and the choice of a plating chemistry and process can impact the number of post-CMP defects. (Data based on 50% die inspection using KLA 2138 tool.)

Because the selection of a CMP slurry is primarily driven by removal rates, dishing and erosion criteria, it is sometimes difficult to make further changes to optimize for mousebite defects. Similarly, the choice of a barrier material is primarily a function of its copper barrier properties as well as adhesion, and thus may be contrary to a selection that would minimize these defects. On the other hand, it has been found that the copper microstructure in the damascene features can have a marked effect on the post-CMP defect count. The "galvanic-corrosion" hypothesis is manifest in this case by the grain orientation in the features that may have a different etch or corrosion rate. In other words, certain grain orientations may be more susceptible to galvanic

corrosion if they have a minimum (critical) dimension compared with neighboring grains, leading to preferential etching or removal.

Again, this hypothesis has not been proven directly, but there are indirect clues to suggest such a mechanism. For example, the choice of a post-plating anneal condition can have an effect on the incidence of these defects, presumably because it results in grain growth. Also, the choice of a plating chemistry and process (current profile) can impact the number of post-CMP defects. Plating conditions that include reverse currents have been shown to create unfavorable conditions that result in higher post-CMP defects than forward-only (dc) currents. Similarly, chemistries that have certain additives also affect the number of post-CMP defects (Fig. 4).

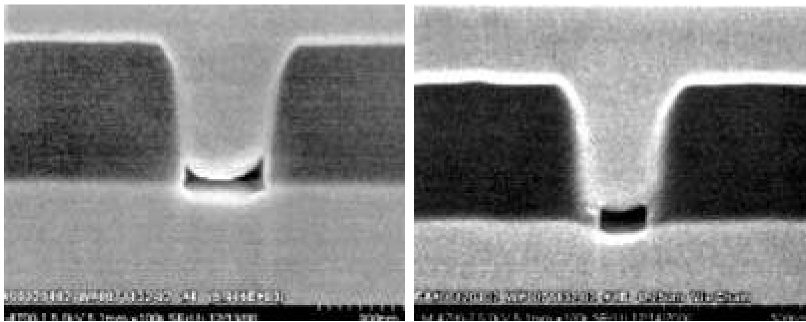


5. Lower temperatures (<200°C) are required to prevent void formation during annealing.

In addition to mousebite defects, it has been observed that the post-plating anneal conditions have a significant impact on overall defects. Higher-temperature anneals lead to within-feature void formation, primarily due to the high rate of change (in microstructure) of the copper overburden relative to the damascene features. Our findings suggest that lower temperatures (<200°C) are required to prevent void formation during annealing (Fig. 5).

On the other hand, it is well known that the copper microstructure within damascene features does not anneal at the same rate as a bulk or thick film. For the damascene features to anneal, either a high temperature or a long time is required. Because high temperature has detrimental effects, the only other parameter is time. If the damascene features are not sufficiently annealed, they will undergo more dramatic stress changes during subsequent thermal cycling, typically resulting in via pullout voids (Fig. 6). As a result, our findings suggest that a low temperature and long time (>30 min) is necessary to prevent anneal-induced voiding and achieve high via-chain yields.

Summary



6. Via pullout voids caused by thermal cycling can result if the damascene features are not sufficiently annealed.

It is important to remember that the number of simultaneous changes required to implement copper interconnects is unprecedented in the history of semiconductor manufacturing. The material (copper), the deposition method (electrofill) and the process flow (damascene) represent significant manufacturing challenges because of their relative infancy. Many manufacturers have significantly underestimated the magnitude of effort required to climb the learning curve and deliver yielding processes. We are only beginning to develop a copper-specific nomenclature in the realm of yield and defects, and we should expect further discoveries as many companies transition into low-k materials combined with copper interconnects.

Author Information

Sesha Varadarajan is process development manager for the Electrofill Products Division at Novellus Systems , and has held a number of positions since joining the company as a process engineer in 1999. He has a bachelor's degree in mechanical engineering from the University of Mysore, and a master's degree in materials science from Boston University.

Dinesh Kalakkad is director of product development for GAMMA 2130 systems at Novellus Systems. He has held several positions since joining the company in 1997, including process engineering manager for the Electrofill Products Division. He has a Ph.D. in chemical engineering from the University of New Mexico.

Theodore Cacouris is director of key account technology for Asia for the Electrofill Products Division. He joined Novellus in 1996 as a member of the Portland Technology Center startup team. He has held several other positions at the company, including senior technologist for copper CVD and electrofill, and marketing director for the Electrofill Products Division. He has a Ph.D. in electrical engineering from Columbia University.

Source : SI,2002/06